first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them;

a third impurity diffusion layer formed in a portion immediately below the gate electrode in the semiconductor substrate; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer.

5. A semiconductor device according to claim 1, wherein an element isolation region is formed in the semiconductor substrate.

9. A semiconductor device according to claim 1, wherein a metal silicide layer is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer on an upper surface thereof.

10. A semiconductor device according to claim 1, wherein the sidewall dielectric layer is formed from a material including, as a main component, silicon nitride, silicon oxide or a compound film thereof.

11. A semiconductor device according to claim 1, wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

12. A semiconductor device according to claim 1, wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and a film thickness that gradually reduces from a bottom thereof toward an upper surface thereof.

Please add the following new claims 21-32:

21. (New) A semiconductor device comprising:

a semiconductor substrate;

a gate electrode formed on the semiconductor substrate through a gate dielectric layer;

first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof,

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and

wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

22. (New) A semiconductor device according to claim 21, wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm.

23. (New) A semiconductor device according to claim 21, wherein a groove section is formed at a specified location in the semiconductor substrate, and the gate electrode is formed on a bottom surface of the groove section through the gate dielectric layer.

24. (New) A semiconductor device according to claim 21, wherein the gate electrode is formed from at least one alloy that includes at least two constituents selected from the following group:

polycrystalline silicon, tungsten, tantalum, copper and gold.

25. (New) A semiconductor device according to any one of claim 21, wherein an element isolation region is formed in the semiconductor substrate.

26. (New) A semiconductor device according to claim 25, wherein the element isolation region is formed from a trench isolation groove and a dielectric layer embedded therein.

27. (New) A semiconductor device according to claim 21, wherein the first and second impurity diffusion layers include an extension region.

28. (New) A semiconductor device according to claim 21, wherein a third impurity diffusion layer is formed in a portion immediately below the gate electrode in the semiconductor substrate.

29. (New) A semiconductor device according to claim 21, wherein a metal silicide layer is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer on an upper surface thereof.

30. (New) A semiconductor device according to claim 21, wherein the sidewall dielectric layer is formed from a material including, as a main component, silicon nitride, silicon oxide or a compound film thereof.

31. (New) A semiconductor device according to claim 21, wherein the sidewall dielectric layer has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and a film thickness that gradually reduces from a bottom thereof toward an upper surface thereof.

32. (New) A semiconductor device comprising:

a semiconductor substrate;

a groove section formed at a specified location in the semiconductor substrate;

a gate electrode formed on a bottom surface of the groove section through a gate dielectric layer;

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and

a width of the upper surface of the gate electrode substantially equals to a width of the groove.